



R22 Regulation

Subject code:4P6DA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular Examinations, May 2025

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 60

Date: 23.06.2025

Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

| All the following questions carry equal marks (10X1M=10 Marks) | | Marks | CO | Bloom Tx |
|--|---|-------|----|----------|
| 1.a) | List the advantages of VLSI technology. | 1M | 1 | 1 |
| b) | What are the keywords used in VHDL. | 1M | 1 | 1 |
| c) | List the Array of Instances of Gate Primitives. | 1M | 2 | 1 |
| d) | Define gate delay. | 1M | 2 | 1 |
| e) | Write Operator Types in Verilog. | 1M | 3 | 1 |
| f) | Compare CMOS switches and bidirectional switches. | 1M | 3 | 2 |
| g) | What are the control statements in Behavioral Modeling. | 1M | 4 | 1 |
| h) | Define Test Benche. | 1M | 4 | 1 |
| i) | Compare between Combinational UDPs and Sequential UDPS. | 1M | 5 | 1 |
| j) | Define Compiler directives. | 1M | 5 | 1 |

Part-B

| Answer All the following questions. (5X10M=50Marks) | | Marks | CO | Bloom Tx |
|---|---|-------|----|----------|
| 2 | Explain the VLSI design flow with the help of neat diagram. | 10M | 1 | 2 |
| OR | | | | |
| 3 | Define Vectors, Scalars and Identifiers with suitable examples. | 10M | 1 | 2 |
| 4 | a) Explain about Tri-state gates in Verilog. | 5M | 2 | 3 |
| | b) Discuss the Net Delays and Gate Delays. | 5M | 2 | 2 |
| OR | | | | |
| 5 | Write Verilog code for 1 to 4 demultiplexer module by using 2 to 4 decoder? | 10M | 2 | 3 |
| 6 | Design half-adder using CMOS switches. | 10M | 3 | 3 |
| OR | | | | |
| 7. | a) Discuss why switch level is useful? | 5M | 3 | 3 |
| | b) Write and verify a switch level al a three-input static CMOS NOR gate? | 5M | 3 | 3 |

| | | | | |
|----|--|-----|---|---|
| 8 | Develop a module and a test bench for a 4-to-1 multiplexer in behavioral model . | 10M | 4 | 3 |
| OR | | | | |
| 9 | Explain the Sequential and Parallel Blocks with suitable examples in behavioral model .. | 10M | 4 | 2 |
| 10 | a) Compare between Tasks and Functions. | 5M | 5 | 3 |
| | b) Explain Compiler Directives and Functions. | 5M | 5 | 2 |
| OR | | | | |
| 11 | What do you mean by user defined primitives (UDP) and explain the types with examples? | 10M | 5 | 3 |